CLAIMS

1. A DMA controller comprising:

at least one peripheral DMA channel for handling DMA transfers on a peripheral access bus;

at least one memory DMA stream, including a memory destination channel and a memory source channel, for handling DMA transfers on first and second memory access buses;

first and second address computation units for computing updated memory addresses for DMA transfers;

first and second memory pipelines for supplying memory addresses to the first and second memory access buses, respectively, and for transferring data on the first and second memory access buses; and

a multiplexer configured to supply first and second current memory addresses to selected ones of the first and second memory pipelines in response to a control signal.

2. A DMA controller as defined in claim 1, further comprising a peripheral prioritizer for prioritizing DMA requests for access to the peripheral access bus and a memory prioritizer for prioritizing DMA requests for access to one or both of the memory access buses.

3. A DMA controller as defined in claim 1, further comprising a traffic controller configured to give preference to consecutive transfers in one direction on one or more of the buses.

4. A DMA controller as defined in claim 1, wherein each of the peripheral DMA channels has a data FIFO with inputs receiving data from the peripheral access bus and the memory access buses and with outputs supplying data to the peripheral access bus and the memory access buses.

5. A DMA controller as defined in claim 4, further comprising an urgent controller configured to increase the priority of a memory transfer when a peripheral DMA request is received and the data FIFO in a corresponding peripheral DMA channel is not ready to transfer data.

6. A DMA controller as defined in claim 4, wherein each of the one or more memory destination channels has a data FIFO with inputs receiving data from the memory access buses and with outputs supplying data to the memory access buses.

7. A DMA controller as defined in claim 1, wherein the multiplexer is configured to receive the first current memory address from one of the peripheral DMA channels or one of the memory destination channels and to receive the second current memory address from one of the memory source channels and to supply the first and second current memory addresses to selected ones of the memory pipelines.

8. A DMA controller as defined in claim 1, wherein each of the memory pipelines includes an address and write data pipeline for supplying memory addresses and write data to the respective buses, a read data pipeline for receiving read data from the respective buses and a control flow pipeline for controlling the flow of control information during a memory access.

9. A DMA controller comprising:

a plurality of DMA channels, each having associated therewith a register file for holding DMA parameters, at least selected ones of said DMA channels including a data FIFO;

a peripheral bus interface for coupling the DMA channels to a peripheral access bus;

a peripheral prioritizer for prioritizing DMA requests for access to the peripheral access bus;

a memory bus interface for interfacing the DMA channels to at least one memory access bus; and

a memory prioritizer for prioritizing DMA requests for access to the memory access bus.

10. A DMA controller as defined in claim 9, further comprising a traffic controller configured to give preference to consecutive transfers in one direction on one or more of the buses.

11. A DMA controller as defined in claim 10, wherein the traffic controller comprises a traffic counter that is loaded with an initial count and means for decrementing the counter on consecutive transfers in one direction, wherein the preference is maintained until the traffic counter decrements to zero.

12. A DMA controller as defined in claim 9, further comprising an urgent controller configured to increase the priority of a memory transfer when a

peripheral DMA request is received and the data FIFO in a corresponding peripheral DMA channel is not ready to transfer data.

13. A DMA controller as defined in claim 9, wherein the peripheral prioritizer arbitrates among DMA requests based on channel number and a traffic control parameter which gives preference to consecutive transfers in one direction on the peripheral access bus.

14. A DMA controller as defined in claim 9, wherein the memory prioritizer arbitrates among DMA requests based on channel number, a traffic parameter which gives preference to consecutive transfers in one direction on the memory access bus and an urgent parameter which gives preference to peripheral requests when the corresponding data FIFO is not ready to transfer data.

15. A DMA controller comprising:

a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination and a control circuit for controlling data transfer through the respective datapath in response to DMA parameters; and

a prioritizer configured to arbitrate among DMA requests, the prioritizer configured to increase the priority of a memory transfer when a peripheral DMA request is received and a corresponding peripheral DMA channel is not ready to transfer data.

16. A DMA controller as defined in claim 15, wherein the prioritizer is configured to set an urgent bit when the peripheral DMA request is received and the corresponding peripheral DMA channel is not ready to transfer data.

17. A DMA controller as defined in claim 16, wherein a memory transfer having the urgent bit set has higher priority than all memory transfers with the urgent bit not set.

18. A DMA controller as defined in claim 16, wherein the prioritizer is configured to arbitrate among memory DMA requests according to a predetermined priority when two or more channels have the urgent bit set.

19. A DMA controller as defined in claim 15, wherein each of the DMA channels includes a data FIFO and wherein the prioritizer is configured to increase the priority of a memory transfer when the corresponding data FIFO is full on receive or empty on transmit.

20. A method for DMA transfer, comprising:

providing a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination and a control circuit for controlling data transfer through the respective datapath in response to DMA parameters;

arbitrating among DMA requests according to a priority associated with each of the DMA channels; and

increasing the priority of a memory transfer when a peripheral DMA request is received and a corresponding peripheral DMA channel is not ready to transfer data.

21. A DMA controller comprising:

a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination on an access bus and a control circuit for controlling data transfer through the respective datapath in response to DMA parameters; and

a prioritizer configured to arbitrate among DMA requests, the prioritizer configured to give preference to consecutive transfers on the access bus in one direction.

22. A DMA controller as defined in claim 21, wherein the prioritizer is configured to eliminate the preference for consecutive transfers in the same direction after a predetermined number of transfers in the same direction.

23. A DMA controller as defined in claim 21, wherein the prioritizer is configured to eliminate the preference for consecutive transfers in the same direction in the absence of DMA transfers in that direction.

24. A method for DMA transfer, comprising:

providing a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination on an access bus and a control circuit for controlling data transfer through the respective datapath in response to DMA parameters;

arbitrating among DMA requests; and

giving preference to DMA requests corresponding to consecutive transfers on the access bus in one direction.